Digital Signals

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W. Bolton, "Mechatronics --- Electronic control systems in mechanical and electrical engineering," 5th edition, Pearson Education Limited 2012, Chap 4
J. Edward Carryer, R. Matthew Ohline, Thomas W. Kenny, "Introduction to Mechatronic Design," Prentice Hall 2011, Chap 16, 19
線上學習網站：https://www.electronics-tutorials.ws
PowerPoint 中部分圖片擷取和修改自教科書和網路圖片

Digital Signals -1

- Function
  - To represent information with logical states
    - True – ON, 1, high – a voltage close to power a device (ex: 5V, 3.3V)
    - False – OFF, 0, low – 0V
    - In a 5V device: -0.3V~1.8V Low ; 3.6V~5.5V High
- Digital devices
  - Logic devices (ex: AND, OR, NOT…)
  - Microcontroller
  - Programmable logic controller (PLC)
  - Sensors / actuators (might be analog as well)

Digital Signals -2

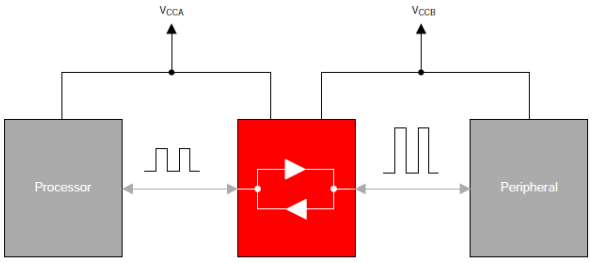
- Timing limitations
  - Input timing:
    - An upper frequency limit to how often an input signal may change states (often a few MHz)
    - Rise time & fall time (10% - 90%)
  - Output timing: Real output exhibit a finite rise time and fall time
  - Delays: A short propagation time occurs as the information propagates through the device
  - Preparation
    - Setup time: Information at an input is required to be present and stable for a minimum amount of time
    - Hold time: the data must remain stable for a minimum amount of time

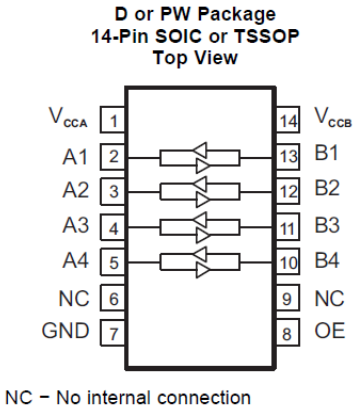
Digital Signals -3

- Pull-ups and pull-downs
  - Floating: when a digital device input is not actively driven by the output of another device; may change states randomly
    - Electrical noise
    - Extra power consumption
  - The circuit should include provisions to establish the desired state
  - Method: Connecting the input with a resistor
    - To power: Pulled up
    - To ground: Pulled down

Digital Signals -4

- Voltage level Translator
  - Solving the incompatibility between different devices supplied by different power domain
  - Ex: TI TXB0104
    - Bidirectional
    - Automatic Direction Sensing
    - 1.2V to 3.6V on A Port
    - 1.65V to 5.5V on B Port
    - $V_{CC\,A} \leq V_{CC\,B}$





NC – No internal connection

Digital Signals -5

- Binary Numbers
  - Bit 0: Least significant bit (LSB)
  - The highest bit: Most significant bit (MSB)
  - Byte: 8 bits

…	2^3	2^2	2^1	2^0
…	bit 3	bit 2	bit 1	bit 0

$15 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$ ⇨ 1111

$12 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$ ⇨ 1100

Digital Signals -6

- Number systems

Binary-coded decimal system ⇩

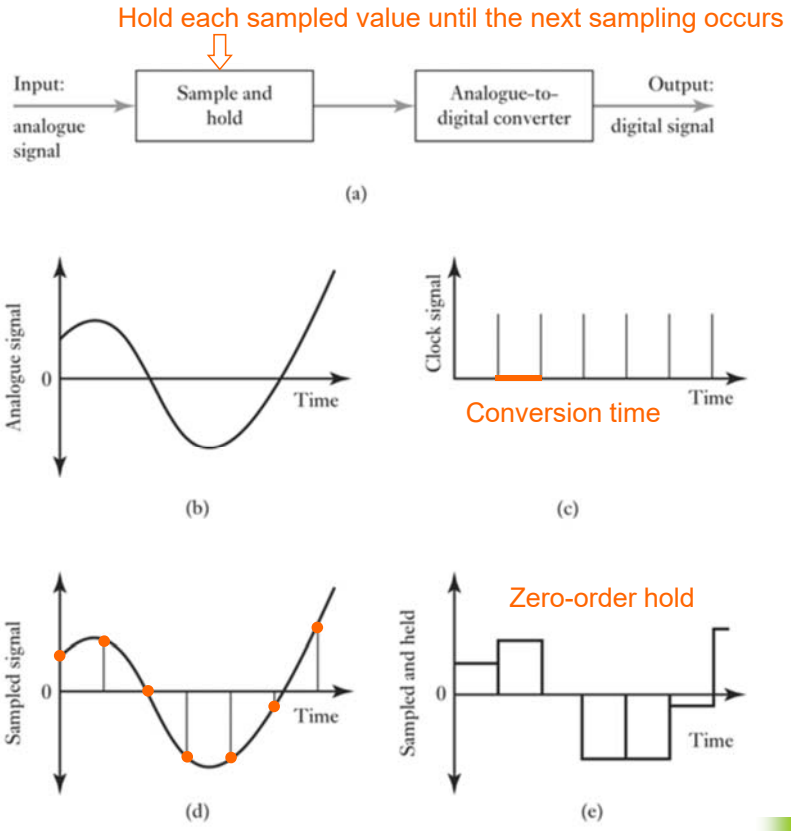
Decimal	Binary	BCD	Octal	Hexadecimal
0	0000	0000 0000	0	0
1	0001	0000 0001	1	1
2	0010	0000 0010	2	2
3	0011	0000 0011	3	3
4	0100	0000 0100	4	4
5	0101	0000 0101	5	5
6	0110	0000 0110	6	6
7	0111	0000 0111	7	7
8	1000	0000 1000	10	8
9	1001	0000 1001	11	9
10	1010	0000 0000	12	A
11	1011	0001 0001	13	B
12	1100	0001 0010	14	C
13	1101	0001 0011	15	D
14	1110	0001 0100	16	E
15	1111	0001 0101	17	F

Digital Signals -7

- Parity method for error detection
  - A parity bit: An extra 0 or 1 bit attached to a code group at transmission to detect the errors which alters the logical level of the signal
  - Ex: 1001 → 1101, using “even” parity bit
    - Add 0 to an even number 01001
    - Add 1 to an odd number 11101
- Checksum
  - A block of code may be checked by sending a series of bits representing their binary sum

Analog and Digital Signals -1

- A-to-D conversion

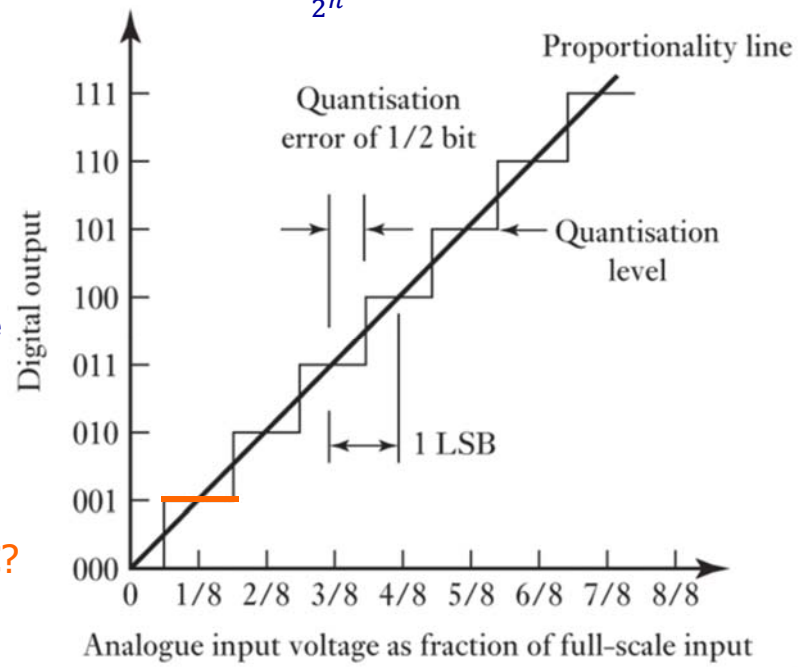


Analog and Digital Signals -2

- A-to-D conversion
  - Analog full scale F_s, n-bit → resolution $\frac{F_s}{2^n}$
- Ex: Thermalcouple
  - $0.5\ \mathrm{mV/°C}$
  - Measurement range

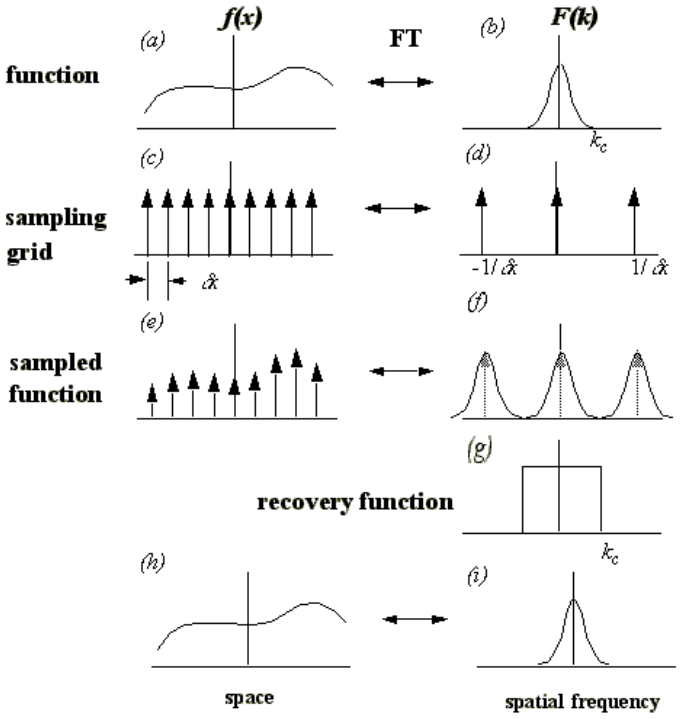
    $0 - 200°C$
  - Resolution $0.5°C$

    ⇨ Need ?-bit ADC?



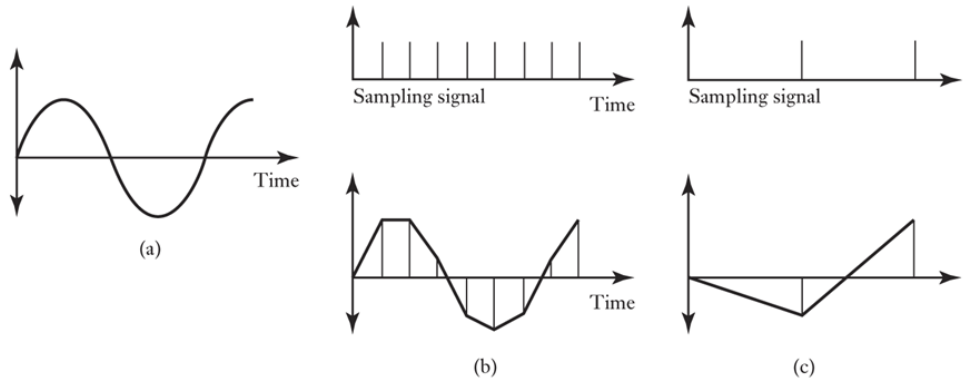
Analog and Digital Signals -3

- Sampling Theorem
  - A continuous time signal can be represented in its samples and can be recovered back when sampling frequency f_s is greater than or equal to the twice the highest frequency f_m component of message signal → $f_s \geq 2f_m$

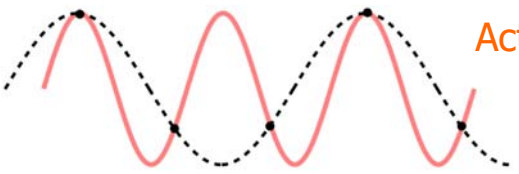


Analog and Digital Signals -4

- Effect of sampling frequency



  - The samples of two sine waves can be identical when at least one of them is at a frequency above half the sample rate



Actual signal

Aliased (apparent) signal

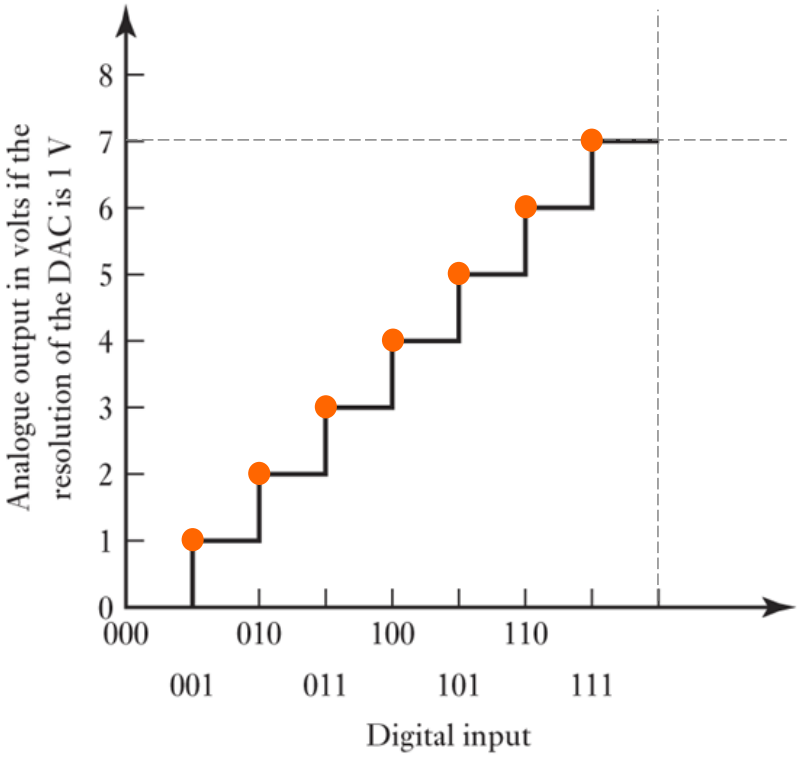
→ Use antialiasing filter (Ex: low-pass)

Analog and Digital Signals -5

- A-to-D conversion errors
  - Quantization error, $\pm\frac{1}{2}LSB$
  - Offset error: the line drawn through the midpoint of each of the steps intersects the x-axis at a location other than the origin
  - Gain error: The slope of the line representing the transfer function differs from the idea slope
  - Nonlinearity error

Analog and Digital Signals -6

- D-to-A conversion

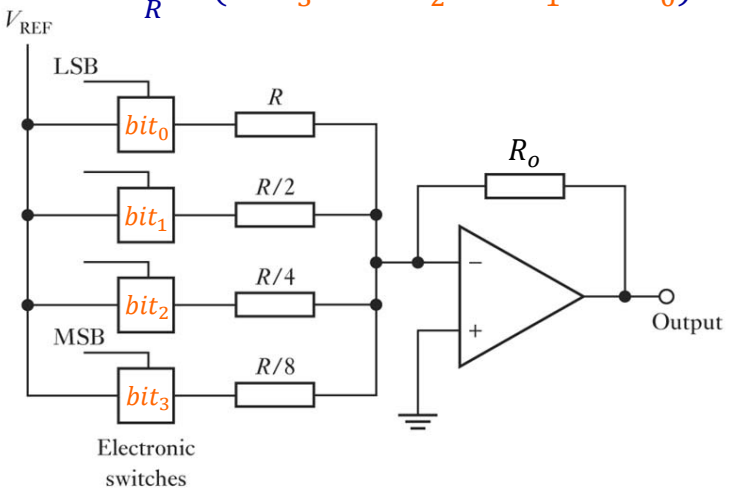


A-to-D and D-to-A converters -1

- PWM DAC
- Weighted-resistor DAC
  - OP summing circuit
  - Ex: 4-bit conversion
  - Drawback:
    - Need accurate resistors over a wide range

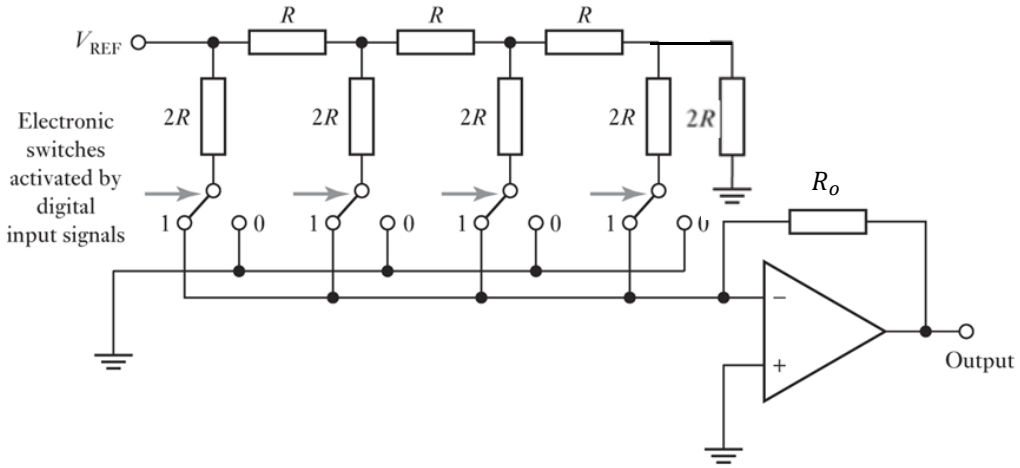
$$V_{out} = -\left(\frac{R_o}{\frac{R}{8}}bit_3 + \frac{R_o}{\frac{R}{4}}bit_2 + \frac{R_o}{\frac{R}{2}}bit_1 + \frac{R_o}{R}bit_0\right)V_{REF}$$

$$= -\frac{R_o V_{REF}}{R}(8bit_3 + 4bit_2 + 2bit_1 + 1bit_0)$$



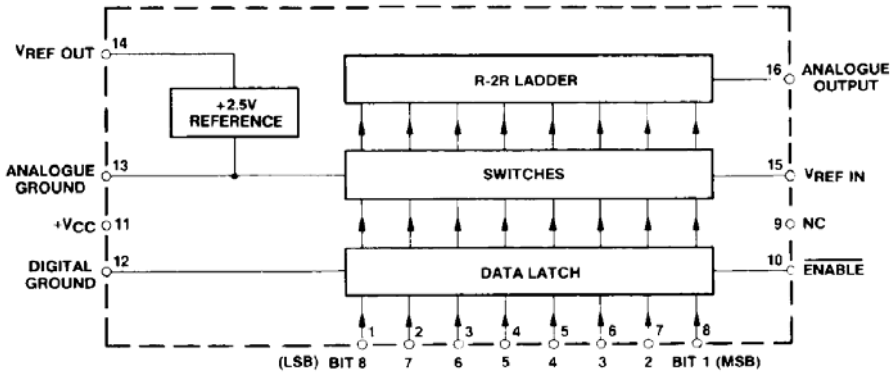
A-to-D and D-to-A converters -2

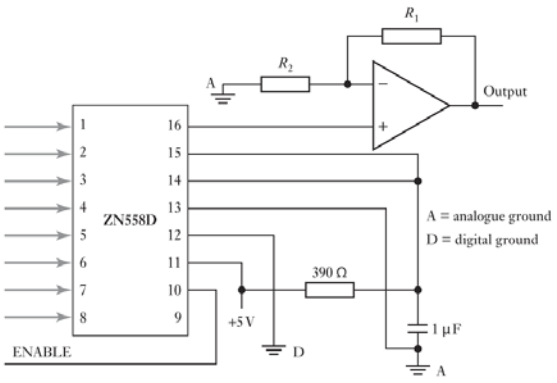
- R-2R ladder DAC
  - Advantages
    - Easily scalable to any desired number of bits
    - Uses only two values of resistors

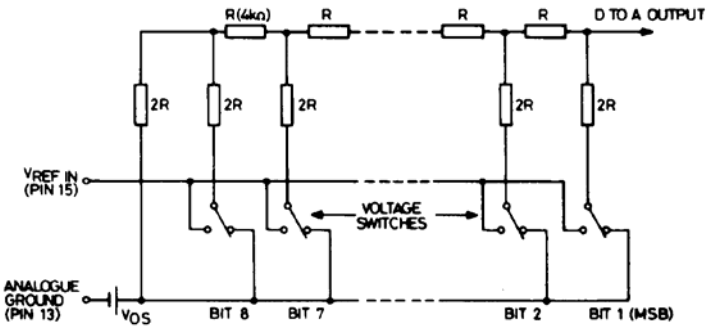


A-to-D and D-to-A converters -3

- Ex: ZN558D

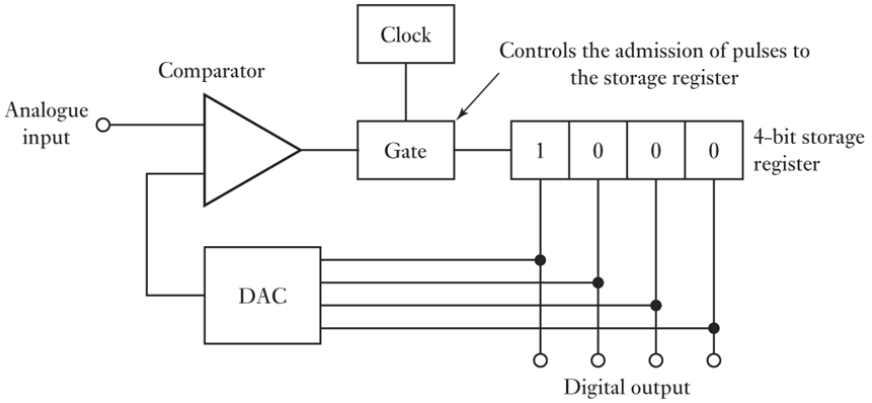






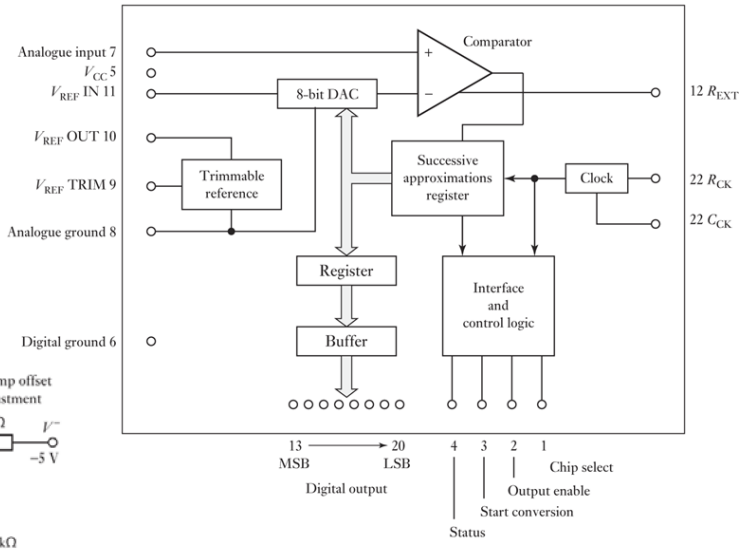
A-to-D and D-to-A converters -4

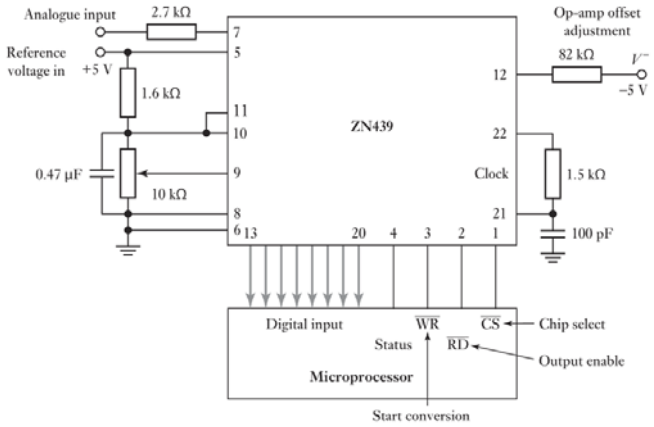
- A-to-D conversion
  - Successive approximation register (SAR)
    - A faster method than the comparison starting the count at 1 and then proceeding but by bit upward
    - n-bit word only takes n steps



A-to-D and D-to-A converters -5

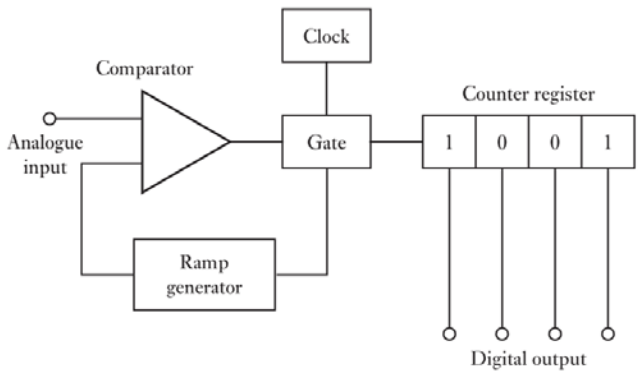
- Ex: ZN439, an 8-bit ADC
  - Conversion time: $5\mu s$



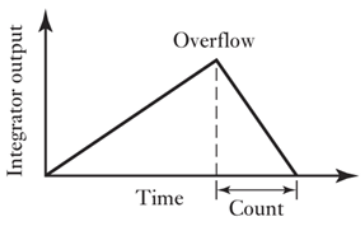


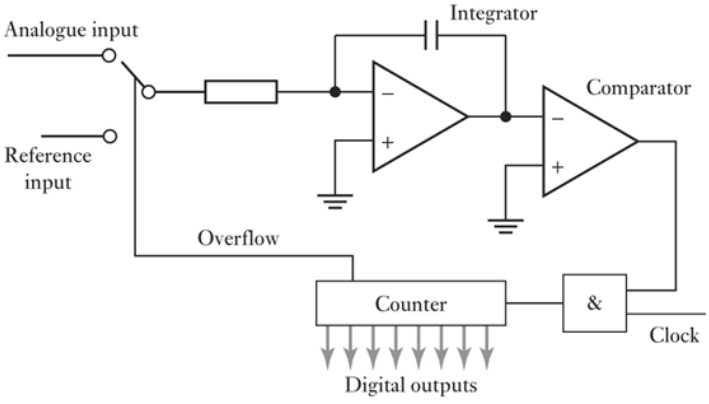
A-to-D and D-to-A converters -6

- Ramp ADC



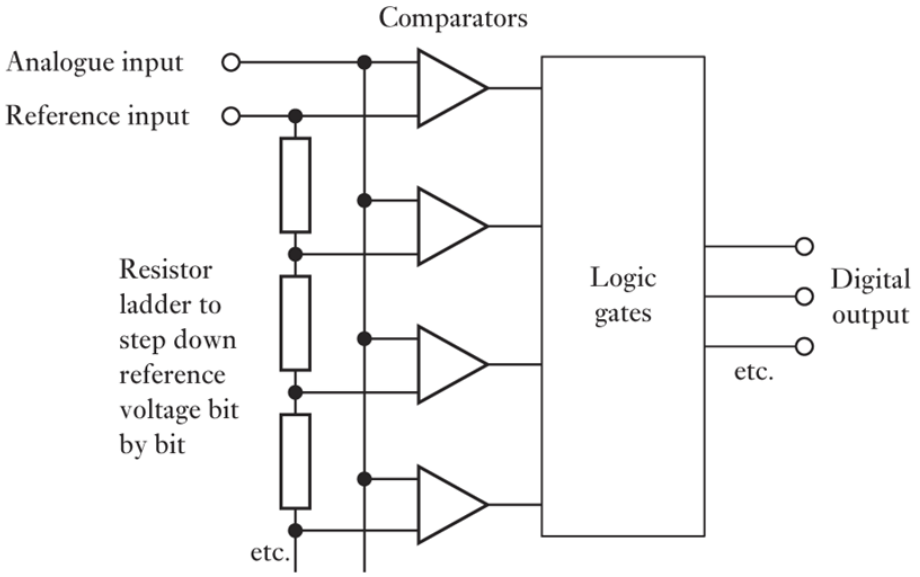
- Dual ramp ADC





A-to-D and D-to-A converters -7

- Flash ADC
  - Very fast: n-bit converter, $2^n - 1$ separate voltage comparators used in parallel

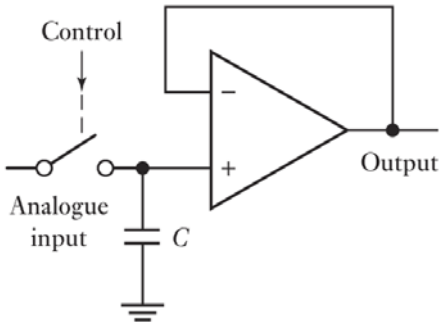


A-to-D and D-to-A converters -8

- ADC specifications
  - Conversion time
  - Resolution
  - Linearity error, $\pm\frac{1}{2}LSB$

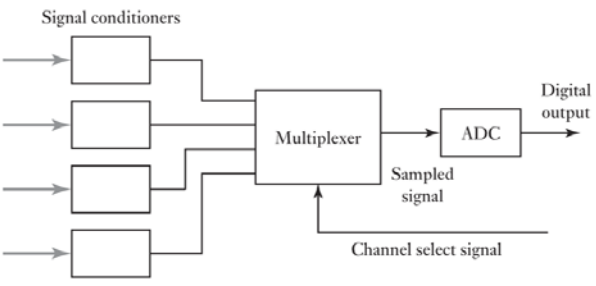
A-to-D and D-to-A converters -9

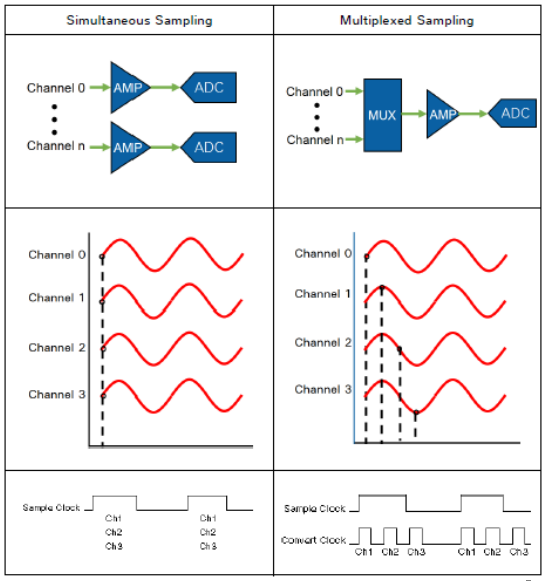
- Sample and hold amplifier
  - To sample the analog signal and hold it while the conversion takes place
  - Switch is closed: $v_{out} = v_{in}$
  - Switch is open: $v_{out} = v_{capacitor}$
  - Acquisition time: the time required for the capacitor to charge to a new sample of the input analog voltage
    - Typical value, $4\mu s$



Multiplexer -1

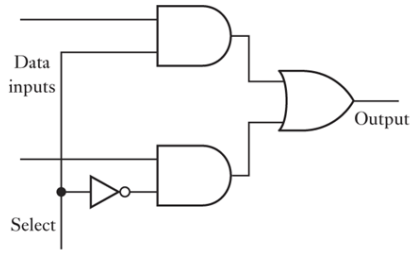
- Multiplexer
  - A device that selects between several analog or digital input signals and forwards it to a single output line
    - AI sampling rate
      - Single channel, Ex: $48\ \mathrm{kS/s}$
      - Multi channels (aggregate)
        - One channel $48\ \mathrm{kS/s}$
        - n channels → $\frac{48}{n}\ \mathrm{kS/s}$



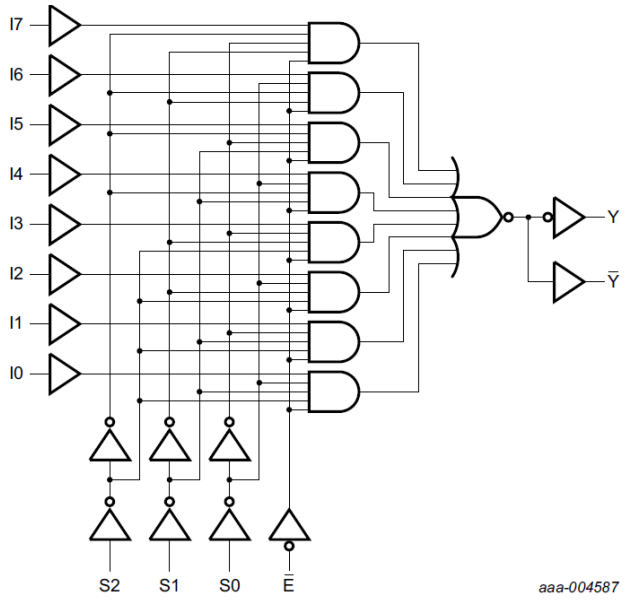


Multiplexer -2

- Digital Multiplexers
  - Ex: a two-input example

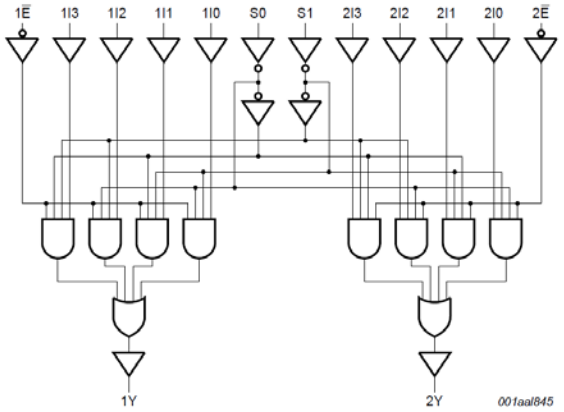


  - Ex: 151 types
    - Enable one line from eight

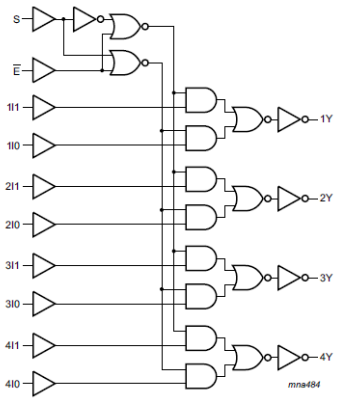


Multiplexer -3

  - Ex: 153 types
    - Enable one line from four inputs which are supplied as data on two lines each

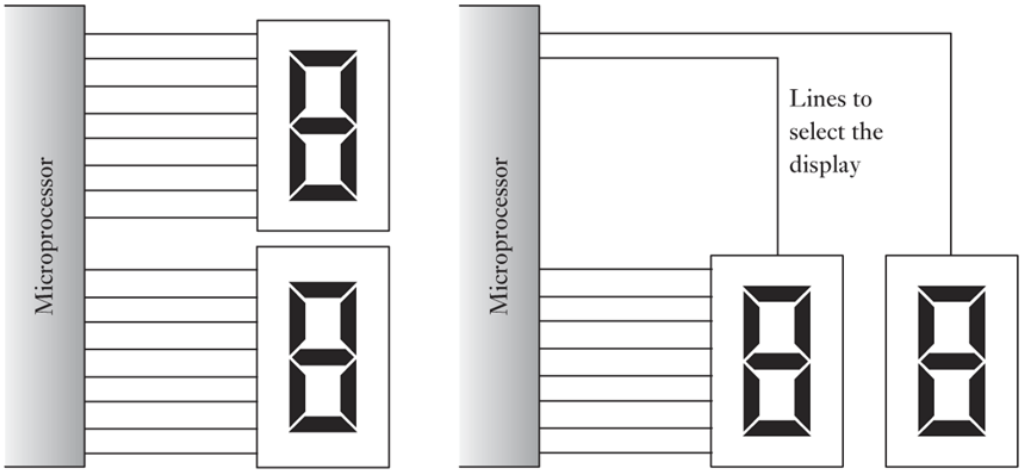


  - Ex: 157 types
    - Enable one line from two inputs which are supplied as data on four lines each



Multiplexer -4

- Time division multiplexer

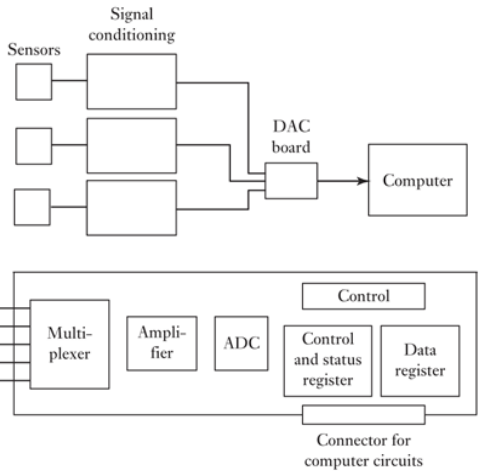


Not time multiplexed

Time multiplexed

Data Acquisition (DAQ)

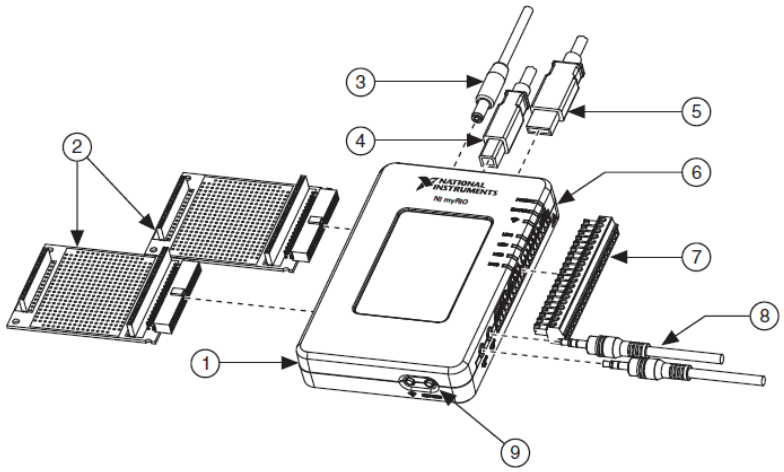
- DAQ
  - Used for the process of taking data from sensors and inputting that data into a computer for processing



- Direct memory access (DMA)
  - A feature of computer systems that allows certain hardware subsystems to access main system memory (random-access memory), independent of the central processing unit (CPU)

NI myRIO 1900 - 1

- Specifications



1	NI myRIO-1900	6	LEDs
2	myRIO Expansion Port (MXP) Breakouts (One Included in Kit)	7	Mini System Port (MSP) Screw-Terminal Connector
3	Power Input Cable	8	Audio In/Out Cables (One Included in Kit)
4	USB Device Cable	9	Button0
5	USB Host Cable (Not Included in Kit)		

NI myRIO 1900 - 2

- Block diagram and connectors

Figure 3. Primary/Secondary Signals on MXP Connectors A and B

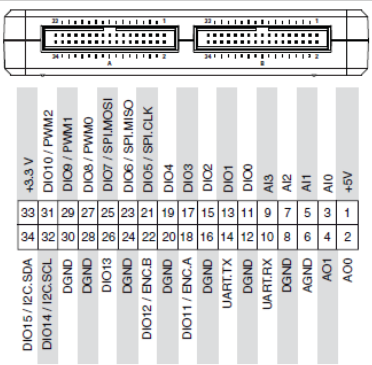
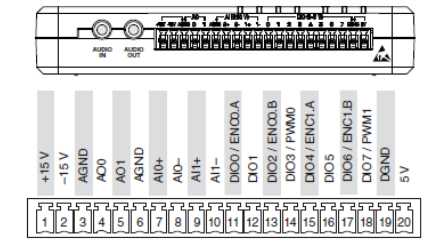
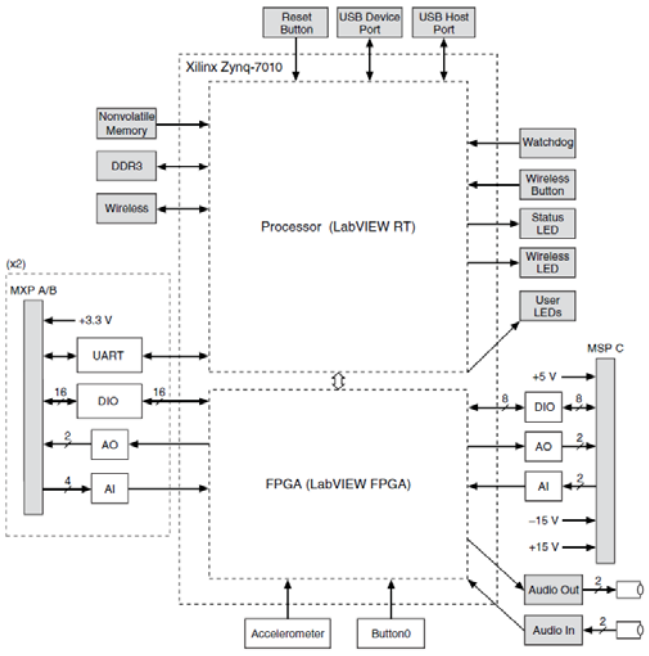


Figure 4. Primary/Secondary Signals on MSP Connector C





NI myRIO 1900 - 3

- Digital IO
  - Channels: 16 (MXP) x2; 8 (MSP)
  - 3.3V output;
  - 3.3V / 5V-compatible input
  - When a DIO line is floating, it floats in the direction of the pull resistor
    - Starting up
    - Configured as input
    - Powering down
  - Secondary digital functions
    - Serial peripheral interface bus (SPI)
    - Pulse-width modulation (PWM)
    - Quadrature encoder input
  - UART TX/RX: identical to DIO 0-13

Figure 7. DIO Lines <13..0> on MXP Connector A or B

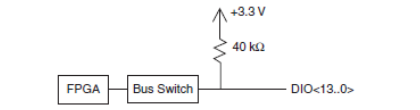


Figure 8. DIO Lines <15..14> on MXP Connector A or B

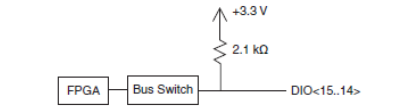
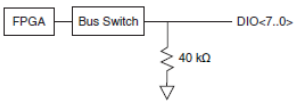
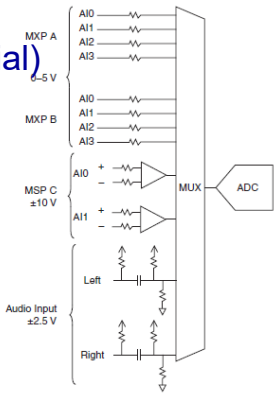


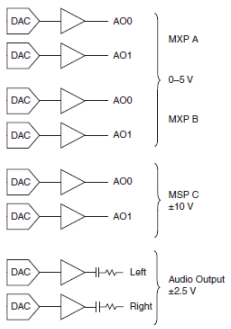
Figure 9. DIO Lines <7..0> on MSP Connector C



NI myRIO 1900 - 4

- Analog input
  - Channels: 4 (MXP, single ended) x2; 2 (MSP, differential)
  - Aggregate sampling rate: $500\ \mathrm{kS/s}$
  - Resolution: $12\ \mathrm{bits}$
  - Nominal range: $0\ V\ \text{ to }\ +5\ V$ (MXP); $\pm 10V$ (MSP)
- Analog output
  - Channels: 2 (MXP) x2; 2 (MSP)
  - Aggregate sampling rate: $345\ \mathrm{kS/s}$
  - Resolution: $12\ \mathrm{bits}$
  - Nominal range: $0\ V\ \text{ to }\ +5\ V$ (MXP); $\pm 10V$ (MSP)
  - Slew rate: $0.3\ \mathrm{V}/\mu s$ (MXP); $2\ \mathrm{V}/\mu s$ (MSP)





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- Questions?